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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,997	08/07/2001	Hiroyuki Takahashi	SIM-01501	1911

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EXAMINER	
COX, CASSANDRA F	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,997	TAKAHASHI, HIROYUKI	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,8,13 and 14* is/are allowed.

6)☒ Claim(s) *1-6,9-12 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicant's arguments with respect to claims 1-6, 9-12, and 15-17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 9-11, and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (U.S. Patent No. 4,970,694).

In reference to claim 1, Tanaka discloses in Figure 7 a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: an inverter chain (34-36) containing not less than one inverter; and a metal-oxide-semiconductor capacitor (40-42), known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter (34-36) and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter, wherein each stage is tied alternately to one of a power voltage source (VDD) and a ground voltage source (VSS). The same applies to claims 2, 16 and 18.

In reference to claim 3, because the claimed structure is fully met by Tanaka, the recited function or "result" limitation "wherein a ratio of a gate voltage range of an on-state MOS capacitor to a gate voltage range of an off-state MOS capacitor is

proportional to an increment or a decrement of the source voltage during a transition period of a signal that appears in the output section of the inverter" will necessarily be inherent in Tanaka, as held by the court in In re Best, 195 USPQ 430. The same applies to claim 9.

In reference to claim 4, because the claimed structure is fully met by Tanaka, the recited function or "result" limitation "wherein a value of the MOS capacitor changes in a direction to increase its capacitance during a transition period of a signal that appears in the output section of the inverter" will necessarily be inherent in Tanaka, as held by the court in In re Best, 195 USPQ 430. The same applies to claims 10 and 17.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 11, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U.S. Patent No. 4,970,694) in view of Hattori (U.S. Patent No. 5,459,424).

In reference to claim 5, Tanaka discloses all of the limitations as mentioned above with reference to claim 1, except that Tanaka does not disclose that the MOS capacitor (40-42) is represented by an n-MOS transistor. Hattori discloses in Figure 1 that the MOS capacitor is disposed on a transmission path of a logic signal, and is

represented by an n-MOS transistor (28) whose gate is connected to a node that changes a logic level of the logic signal from a low level to a high level, and whose source and whose drain are fixed at a ground potential (GND). It would have been obvious to one of skill in the art at the time of the invention that the MOS capacitors (28) of Hattori could be used in place of the MOS capacitor (40-42) of Tanaka as an example of one way of implementing a MOS capacitor. Since Tanaka does not disclose the type (n-type or p-type) of the MOS capacitors (40-42) used in the circuit any type could be used dependent on the particular type of environment. The same applies to claim 11.

In reference to claim 15, Tanaka discloses all of the limitations as mentioned above with reference to claim 2, except that Tanaka does not disclose that the inverter (34-36) is comprised of an n-MOS transistor and a p-MOS transistor. Hattori discloses in Figure 1 an inverter chain (21, 22) containing not less than one inverter; and a p-channel metal-oxide-semiconductor transistor (23) and an n- channel metal-oxide-semiconductor transistor (24), known as MOS transistors, to comprise the inverter (see column 1, lines 20-32), wherein a gate threshold voltage of each gate is shifted in mutually opposing directions. It is well known in the art that inverters can be implemented using a p-MOS and an n-MOS transistor. Therefore, it would have been obvious to one skilled in the art at the time of the invention that the inverter (34-36) of Tanaka could have designed using the method of Hattori as an alternate way of designing an inverter.

5. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U.S. Patent No. 4,970,694) in view of Porter et al. (U.S. Patent No. 6,040,713).

In reference to claim 6, Tanaka discloses all the limitations of the claim as mentioned above with reference to claim 1 except that Tanaka does not disclose that the MOS capacitor is represented by a p-MOS transistor. Porter discloses in column 6, lines 39-45 that the MOS capacitor (92, 94, 96, 98, 100) could also be represented by a p-MOS transistor whose gate is connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose source and drain are fixed at a ground potential. It would have been obvious to one of skill in the art at the time of the invention that the MOS capacitors (92, 94, 96, 98, 100) of Porter could be used in place of the MOS capacitor (40-42) of Tanaka as an example of one way of implementing a MOS capacitor. Since Tanaka does not disclose the type (n-type or p-type) of the MOS capacitors (40-42) used in the circuit any type could be used dependent on the particular type of environment. The same applies to claim 12.

Allowable Subject Matter

6. Claims 7-8 and 13-14 are allowed.

7. The following is an examiner's statement of reasons for allowance: Claims 7 and 13 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the MOS capacitor is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source voltage in

combination with the rest of the limitations of the base claims and any intervening claims. Claims 8 and 14 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the MOS capacitor is represented by a p-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a ground potential in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC
CC
October 4, 2002

Kenneth Wells
Kenneth B. Wells
Primary Examiner